

# Digital Equalization of mmWave Analog Frequency Up and Down-converters

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## 1. Introduction

It is a known fact that time-interleaving of Analog-to-Digital Converters (ADC) is used to increase sampling rate of modern high-performance digitizers. For example, the new 10-bit digitizers from Guzik Technical Enterprises (GTE) feature Keysight Technologies ADC Integrated Circuit (IC), where 160 individual ADC are interleaved to achieve sampling at up-to 64 Gsa/s (160 “slices” sampling at 400 Msa/s) forming two analog channels at 32 Gsa/s each. Time-interleaving that many ADCs makes it challenging to achieve high Spurious-Free Dynamic Range (SFDR). Patented digital equalization technology<sup>1</sup> is used to reduce mismatch between slices, non-flatness of Frequency Response (FR) and Group Delay (GD)<sup>2</sup> of the Digitizer, to create a calibrated baseband receiver in DC -10 GHz band with input signal range from -32 dBm to +22 dBm. The same technology can be extended to equalize FR and GD of Up and Down-converters which are working together with the digitizer to create desired “reference calibration plane” at the Down-converter input (RF reference plane) or at the Up-converter input (IF reference plane).

## 2. 28 GHz frequency band Down-converter FR and GD measurement setup

The simplified block diagram of measurements is shown on Fig. 1

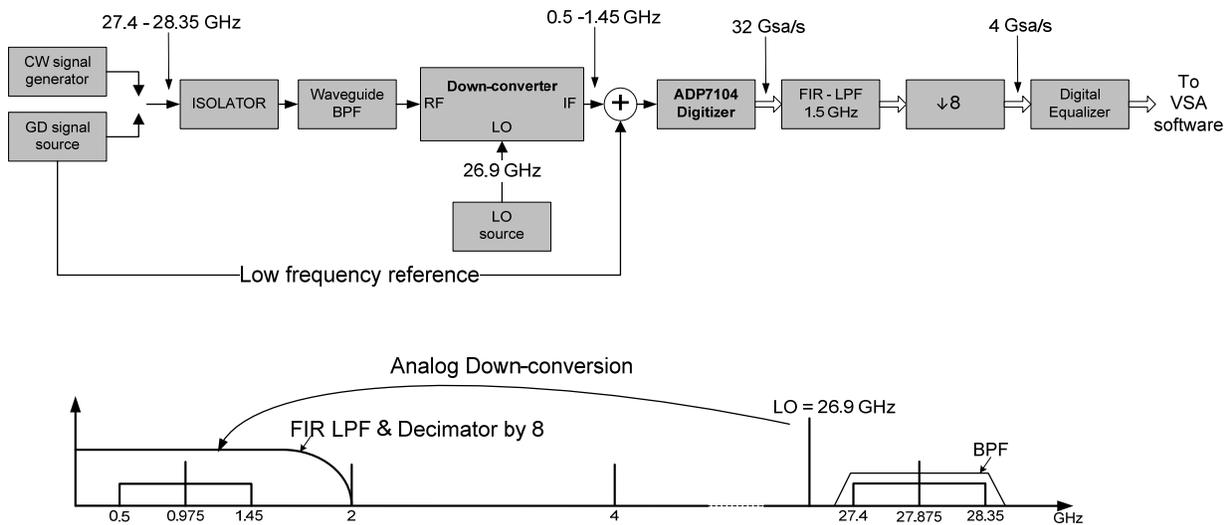


Fig. 1

FR measurement is relatively simple procedure: signal from CW generator is applied through the waveguide Band Pass Filter (BPF) to Down-converter RF input. The measurements are performed in BPF bandwidth of 27.4 – 28.35 GHz. The frequency steps of CW generator were chosen small enough to measure details of the frequency response. About 1200 measurements with frequency step 1 MHz was conducted.

Note: An analog sinewave signal generator with NIST traceable calibration was used to measure the frequency response.

<sup>1</sup> US Patent 7,408,495 Digital Equalization of multiple interleaved Analog-to-Digital converters

<sup>2</sup> US Patent 9,933,467 Group Delay Measurement Apparatus and Method

The Digitizer has been calibrated and FR and GD have been equalized prior to these experiments. To measure GD a GTE proprietary signal source was used. The measured FR and GD are shown on Fig. 2 and Fig. 3 respectively. On the same figures the equalized FR and GD are shown for 1279 tap equalizer. The typical non-flatness of FR and GD are  $\pm 0.1$  dB and  $\pm 100$  ps respectively.

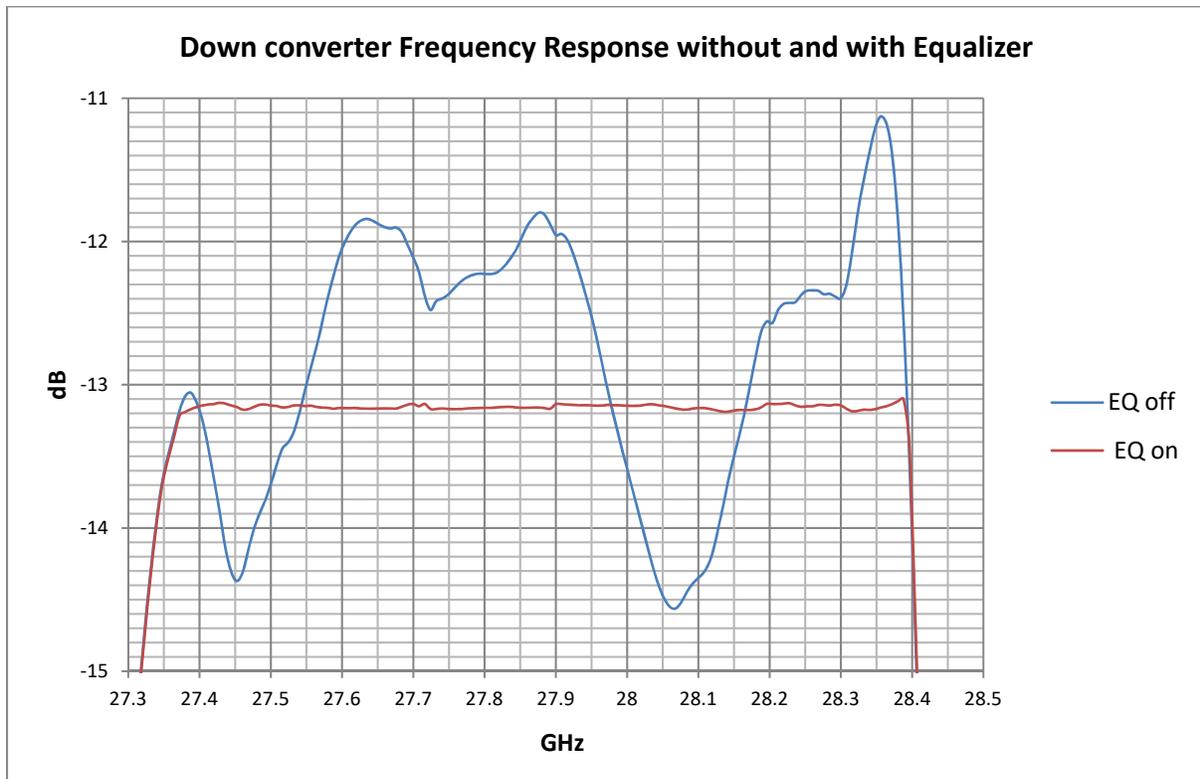


Fig. 2

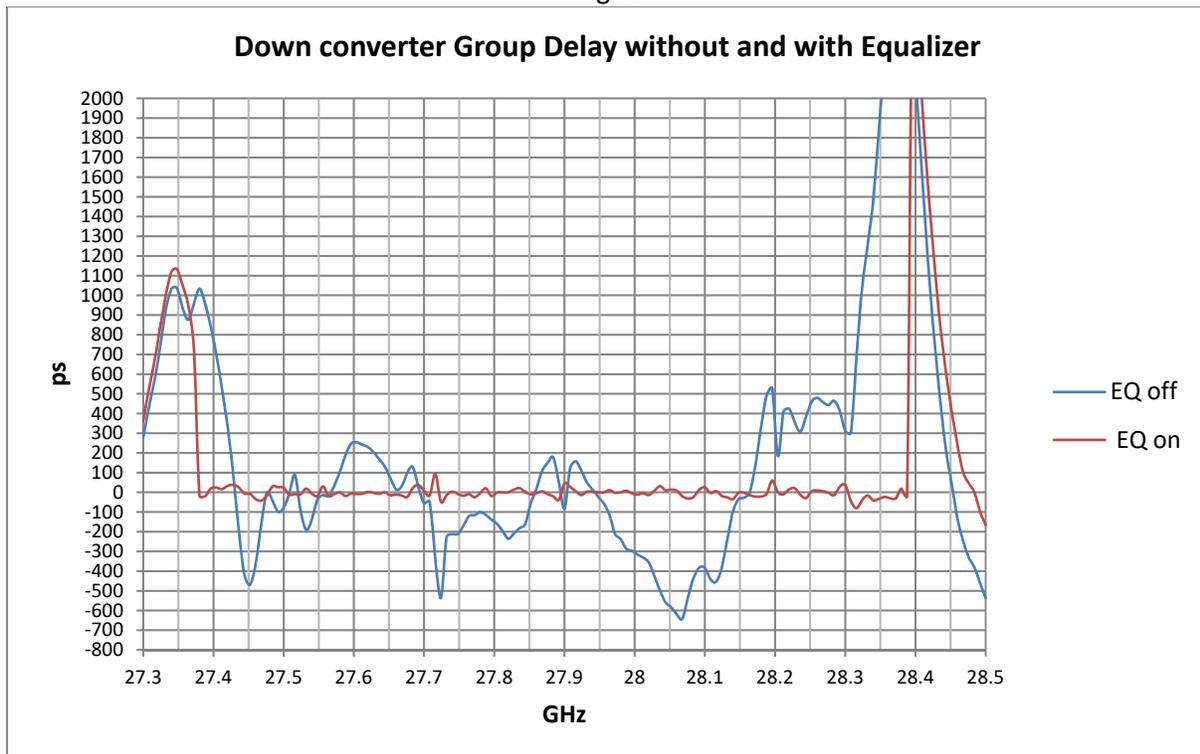


Fig. 3

Below the FR and GD temperature stability of the Down-converter is plotted. The deviation from equalized FR and GD are shown on Fig. 4 and Fig. 5 respectively.

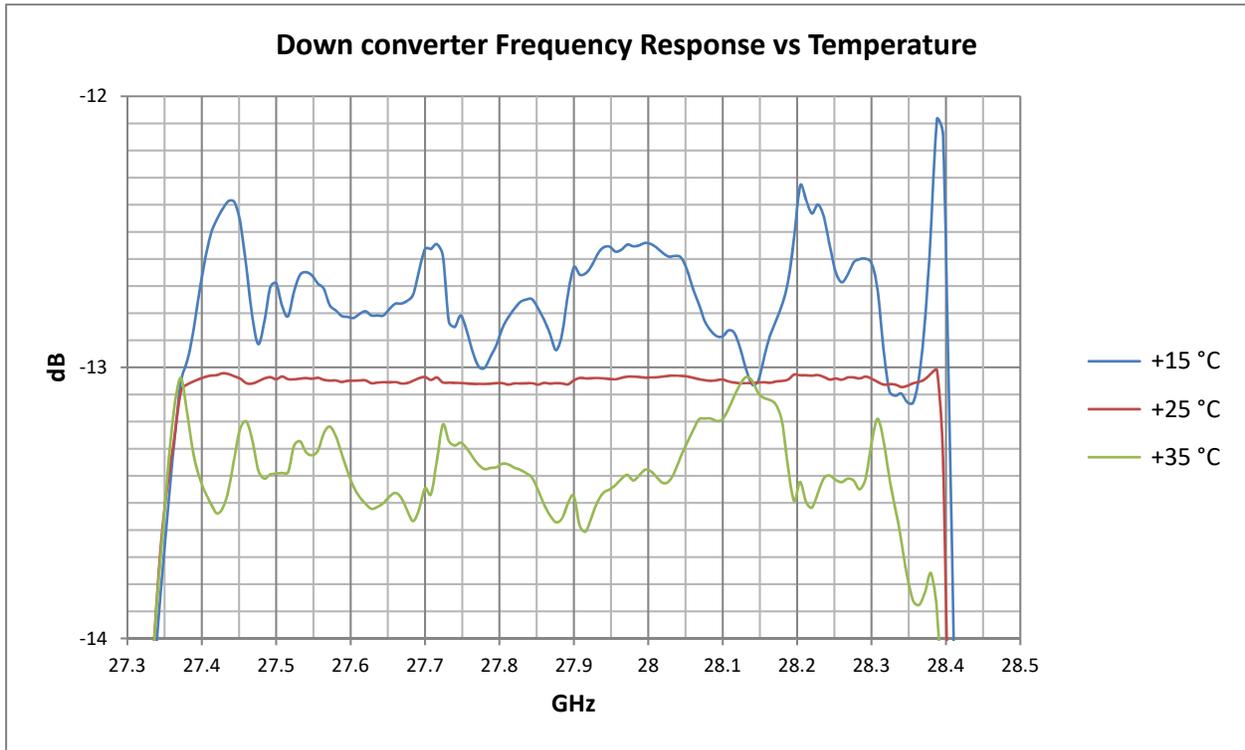


Fig. 4

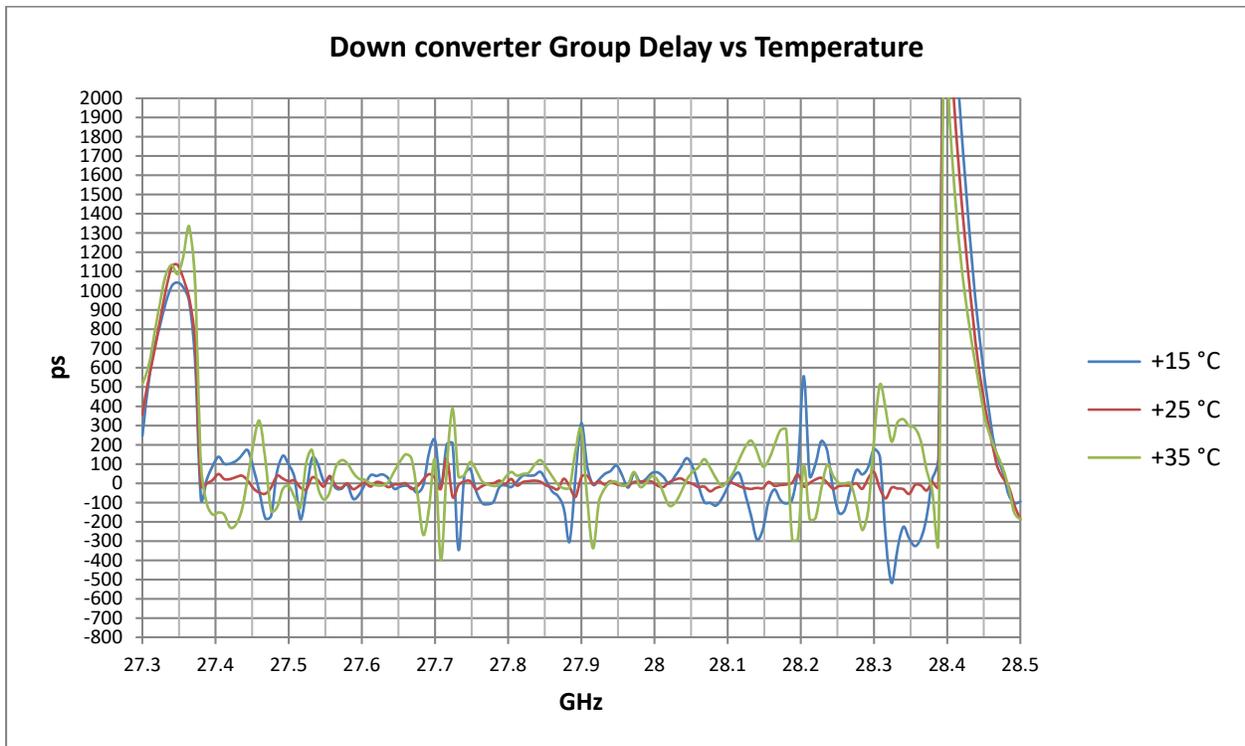


Fig. 5

A Vector Signal Generator (VSG) with low enough base Error Vector magnitude (EVM) in 28 GHz frequency range could not be identified on the market, which made it impossible to measure EVM of the Down-converter before and after equalization. For that reason, the calibration plane was moved to the IF input of the Up-converter.

### 3. 28 GHz frequency band UP and Down-converter FR and GD measurements

The simplified block diagram of measurements is shown on Fig. 6

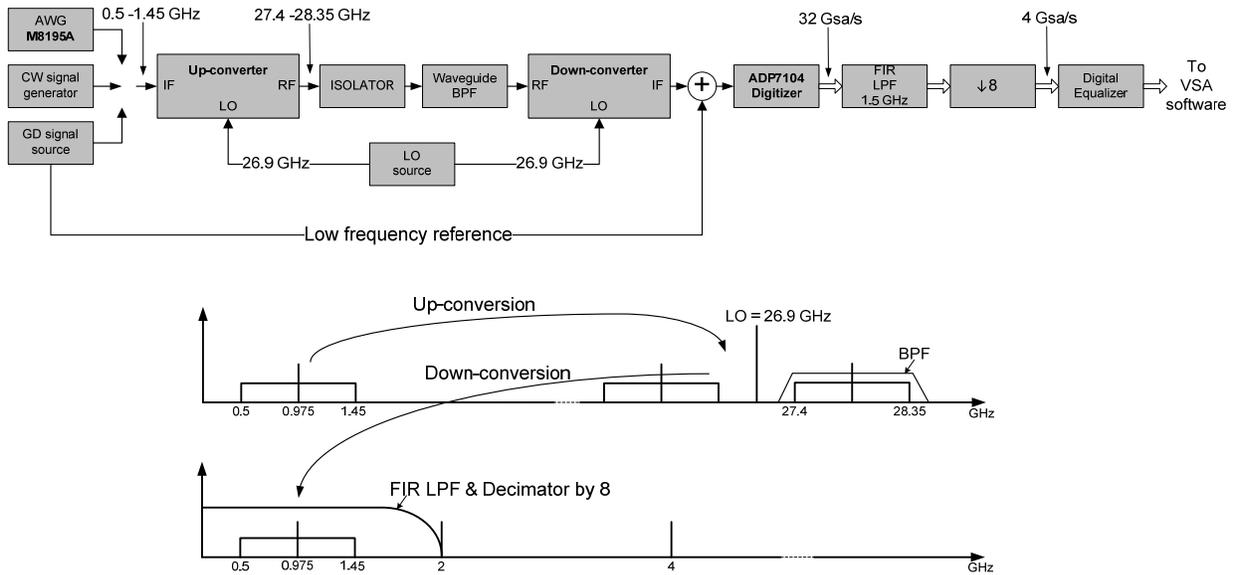


Fig. 6

The CW and GD signals were generated in frequency range 500 MHz to 1.5 GHz such a way that upper sideband at UP-converter output was in the BPF passband (Fig. 6). The measurement results of FR and GD are shown on Fig. 7 and Fig. 8 respectively. On the same figures the equalized FR and GD are shown for 1279 taps equalizer. The typical non-flatness of FR and GD are  $\pm 0.1$  dB and  $\pm 50$ ps respectively.

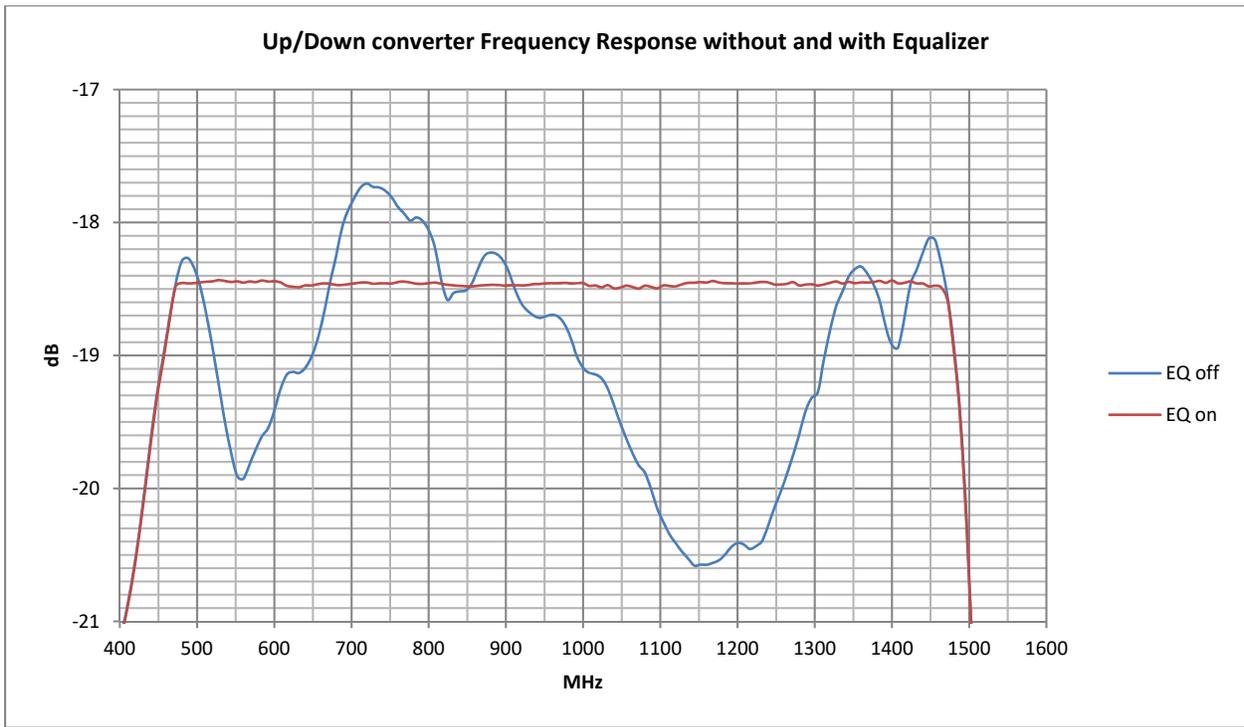


Fig. 7

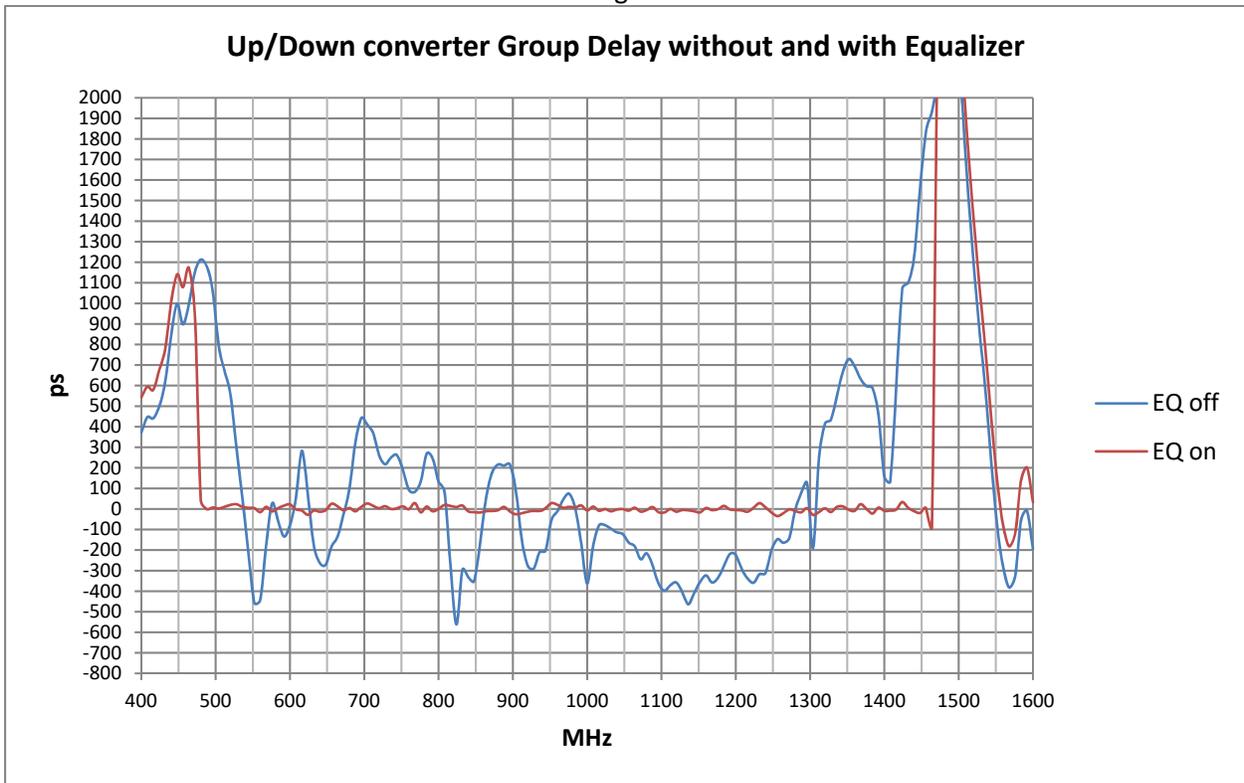


Fig. 8

Fig. 9 and Fig. 10 show how the equalized FR and GD responses are changing with different equalizer number of taps.

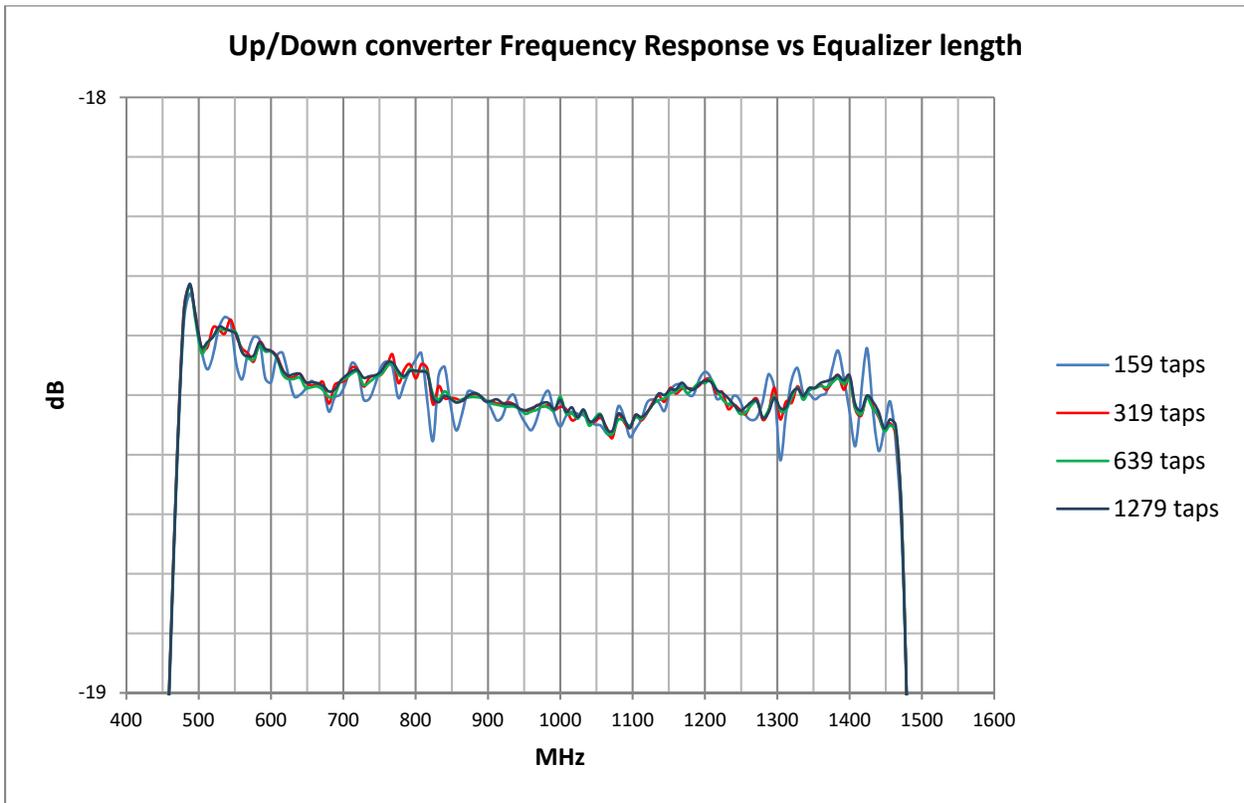


Fig. 9

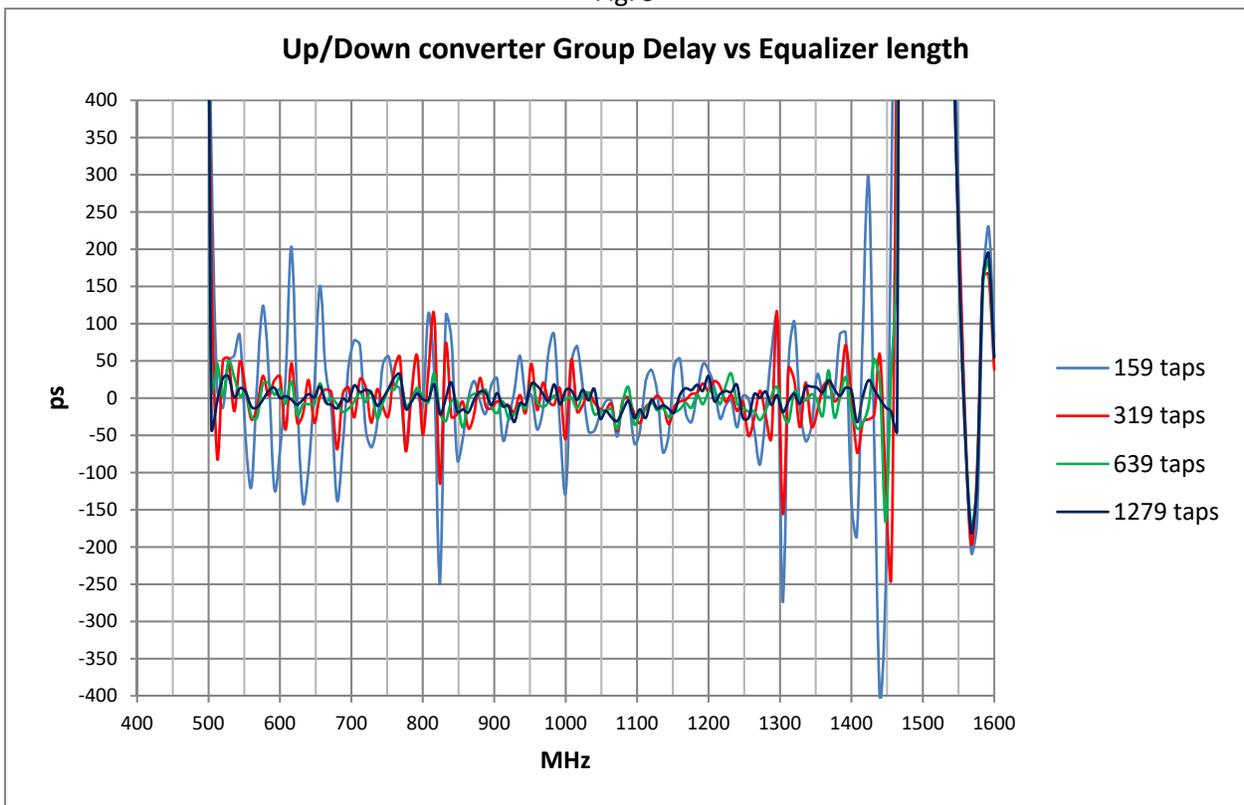


Fig. 10

Fig. 11 and Fig. 12 shows the deviation of equalized FR and GD of UP/DOWN converters for different temperature.

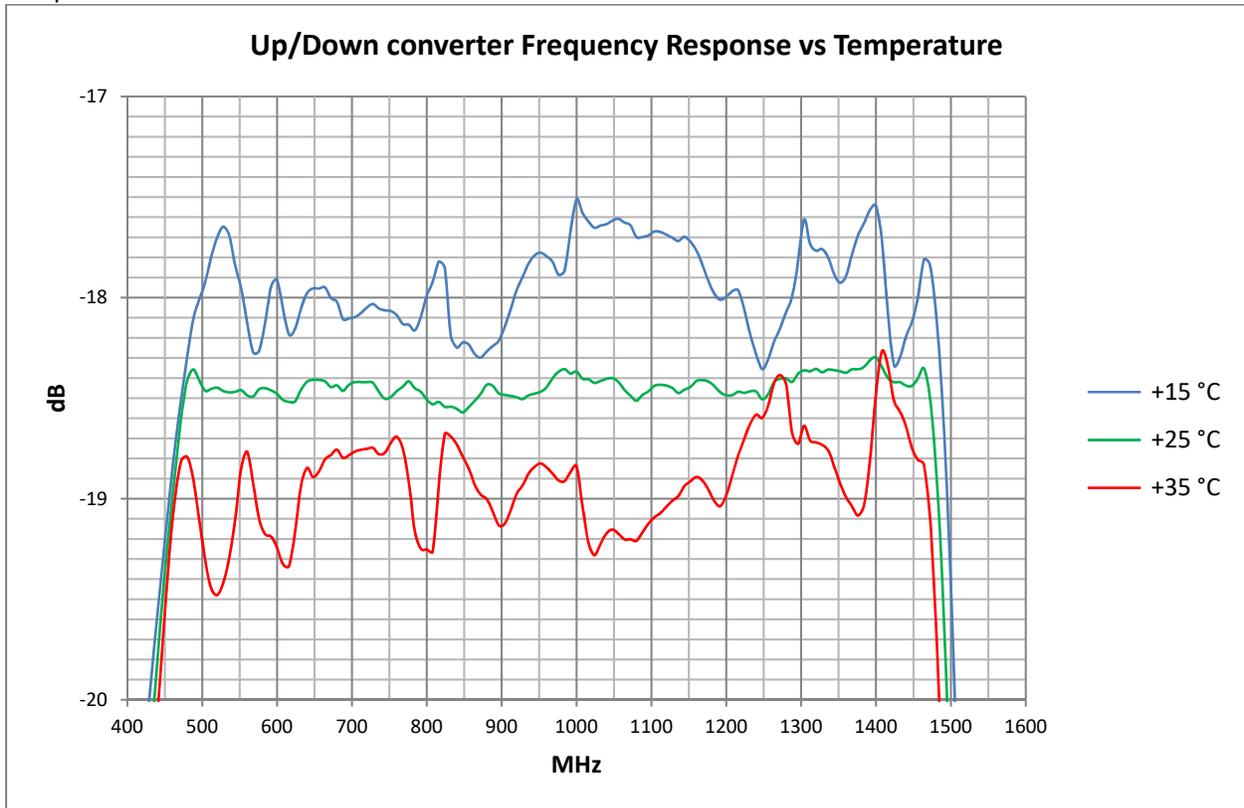


Fig. 11

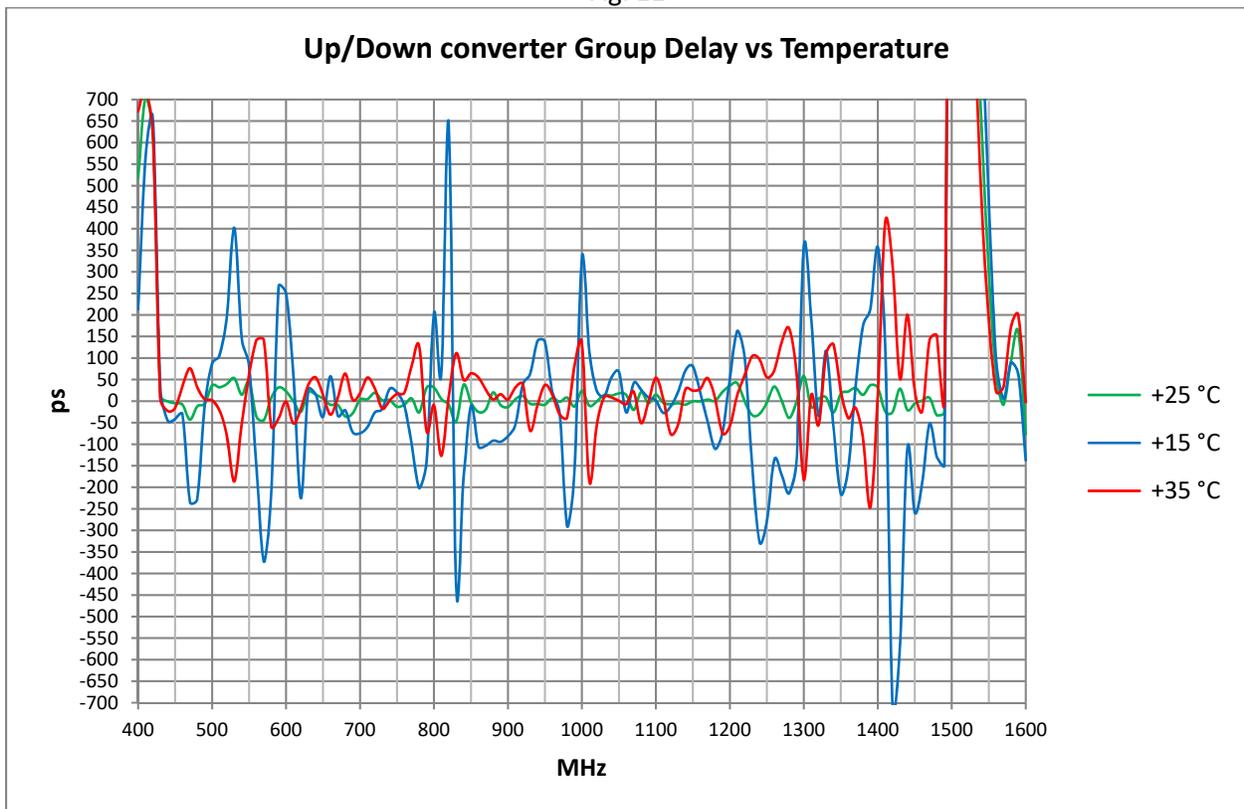


Fig. 12

The results of the EVM measurements for 16QAM and 64QAM, 625 Msymbol/s modulated signal with Root-Raised-Cosine (RRC) filter roll-off factor of 0.35 for transmit and measurement without and with FR and GD equalization are shown on Fig. 13, Fig. 14, Fig. 15 and Fig. 16 using Keysight Technologies VSA 89600 Software. Before equalization EVM is ~11% and after the equalization is ~1% for 16QAM. For 64QAM measured EVM is 8.79% before equalization and ~1% after equalization. The measurements of EVM for different equalizer taps shows that even for 159 taps equalizer EVM is ~1%. Longer equalizer might be needed for wider band Up and Down-converters.

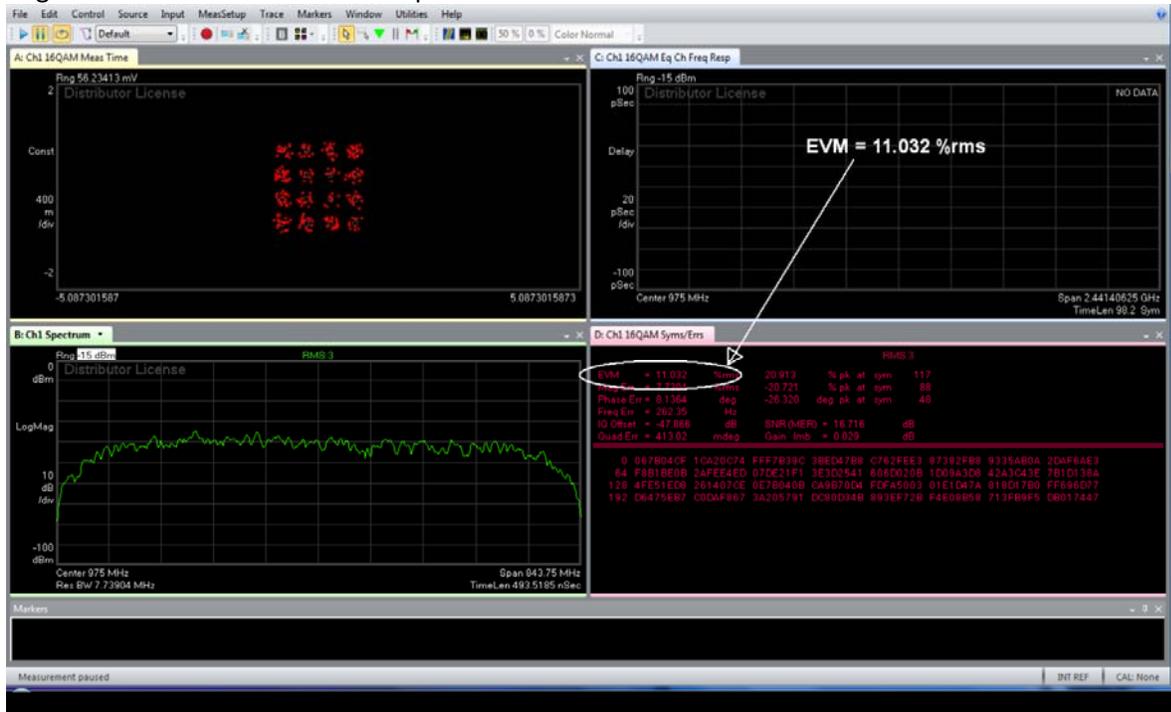


Fig. 13 EVM 16QAM without equalization

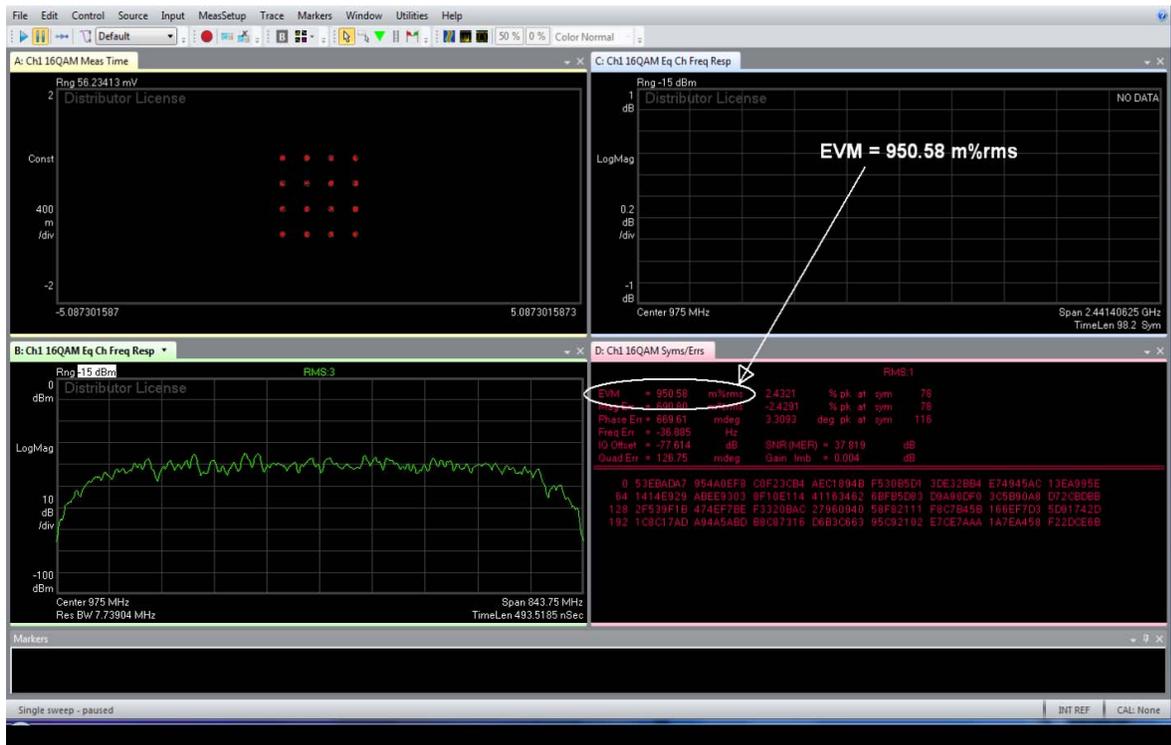


Fig. 14 EVM 16QAM with equalization

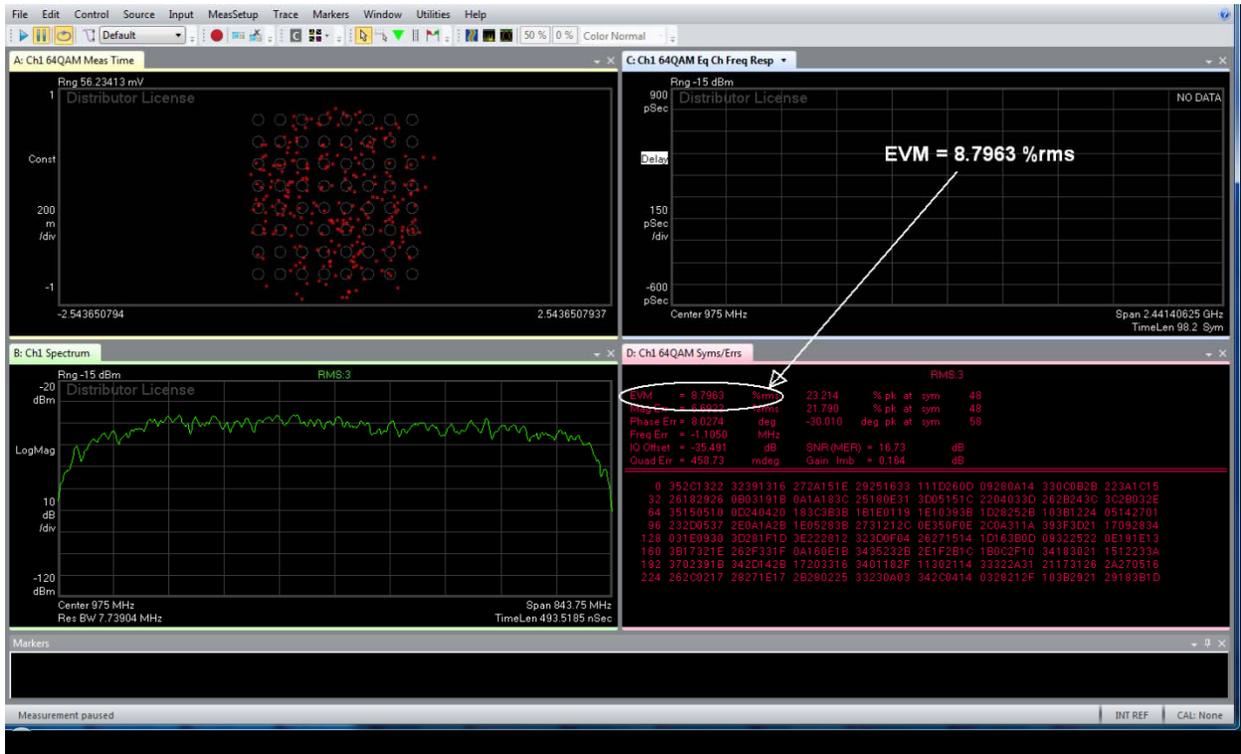


Fig. 15 EVM 64QAM without equalization

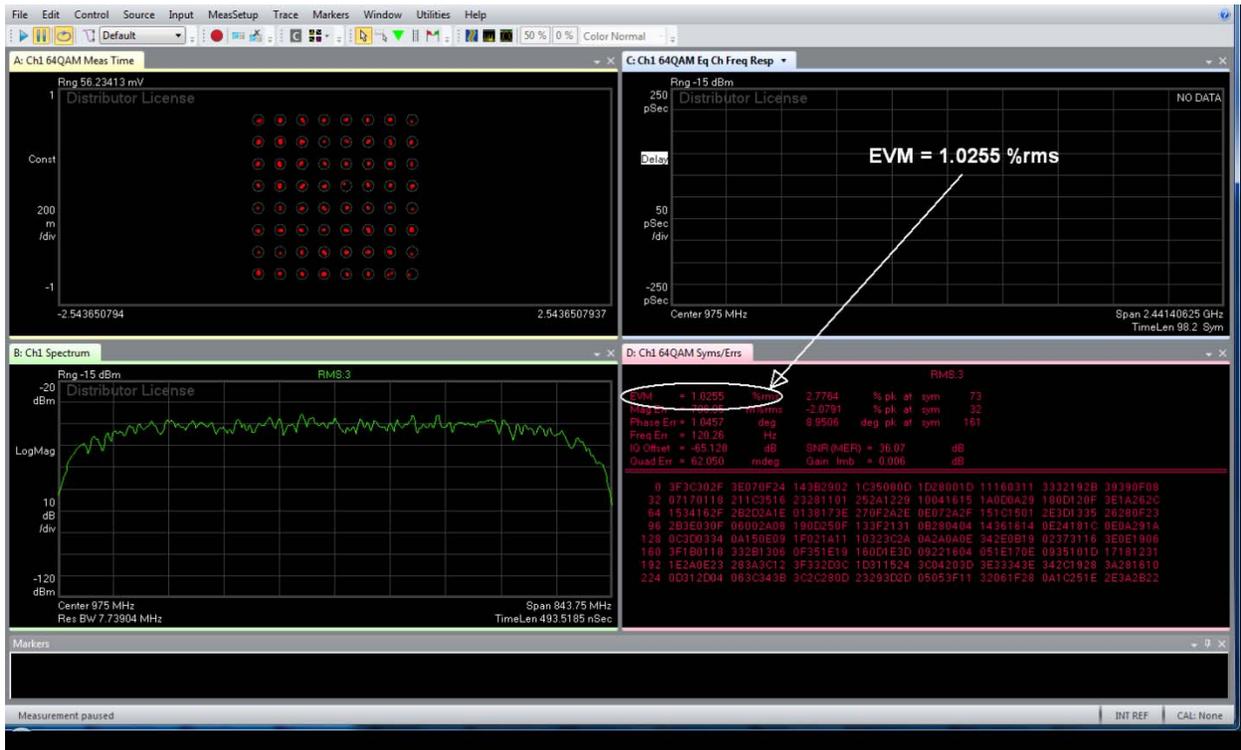


Fig. 16 EVM 64QAM with equalization

Fig. 17 shows how EVM changes over temperature for the Up and Down-converters from ambient calibration temperature +25 °C.

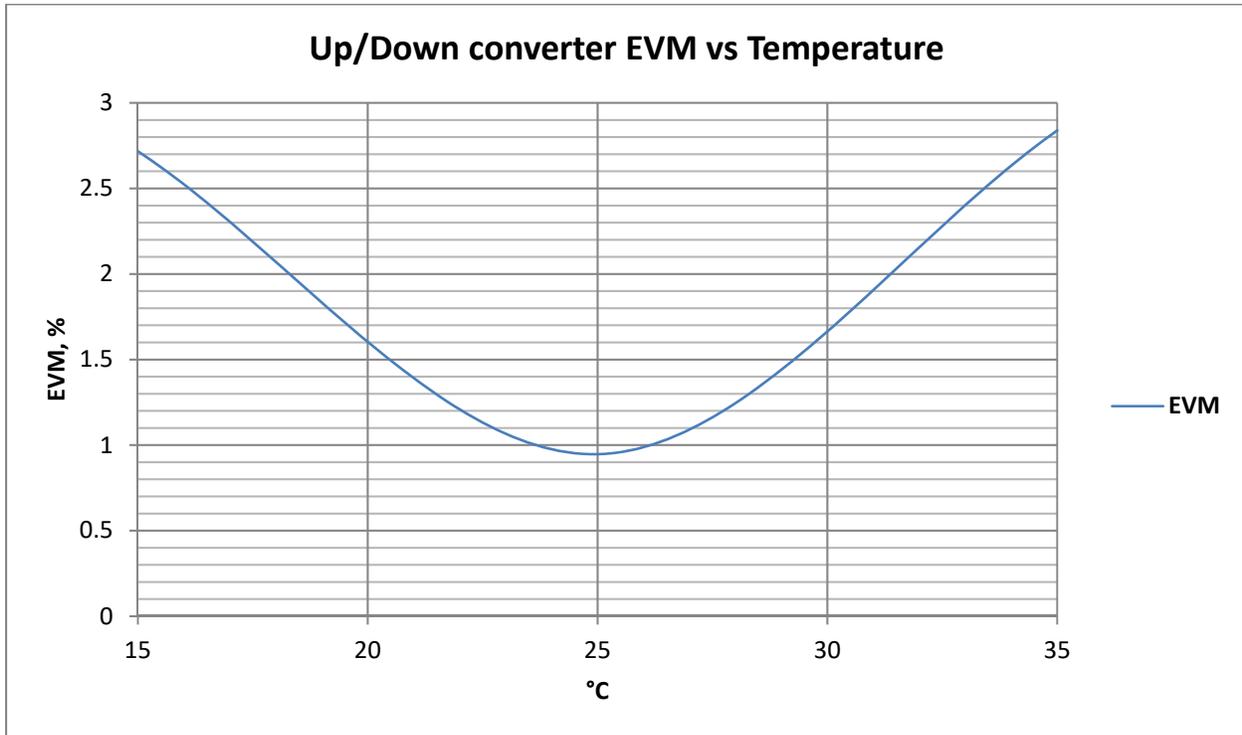


Fig. 17

#### 4. Conclusion

The digital equalization technology based on FR and GD measurements of Up and Down-converters allows to significantly reduce the linear distortions of the test system.

Non-flatness of the FR of the Up and Down-converters was reduced from  $\pm 1.5$  dB to  $\pm 0.1$  dB. Non-flatness of GD was reduced from  $\pm 1.25$  ns to  $\pm 100$  ps. As a result, the residual EVM through the Up/Down-converters in the experiments conducted was reduced from  $\sim 11\%$  (-20 dB) to  $\sim 1\%$  (-40 dB) for 16QAM, 625 Msymbol/s signal with Root-raised-cosine filter (RRC) factor of 0.35, in the 28 GHz band.

The combination of Down-converters and the Digitizer with equalizer can be used to create reference calibration RF reference plane. Thus forming a calibrated reference receiver in mmWave bands up-to 30 GHz, with known FR and GD response. It should be noted that temperature stabilization should be added to the analog Up/Down-converters to achieve repeatability and high accuracy.

The equalization can be done in hardware inside the FPGA-based Digital Processor of the Guzik ADP7000 Series Digitizers in real-time for signals with bandwidth up to 2.5 GHz using the patented<sup>3</sup> Digital Downconverter (DDC). Up-converter (WR28CCU) and Down-converter (WR28CCD) were provided by Virginia Diodes, Inc. for experiment and demonstration purposes of the technology.

<sup>3</sup> US Patent 9,634,679 Digital Down Converter with Equalization